SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to solid state integrated circuit devices and more particularly to [an] improved, miniaturized semiconductor integrated circuit devices.

2. Description of Related Art

Shockley, Bardeen, and Brattain invented the transistor around 1950 and started the modern electronics age. Kilby and Noyce next combined active and passive components on a single chip and invented the integrated circuit. Fairchild's Isoplanar technology (Fig. 1) made possible medium-scale and larger-scale integrated circuits in 1972 according to Peltzer's patent No. 3,648,125. Simultaneously, other similar dielectric isolation processes such as Kooi's LOCOS (i.e., local oxide isolation technology) of Philip and Magdos's oxide-recessed technology of IBM were also widely used. In a 1976 Interference No. 98,426, Li's application No. 154,300 on round-bottomed isolating oxide groove was considered as the "Seniormost Inventor" having the earliest effective filing date of September 23, 1968 among Fairchild's Peltzer, Philip's Kooi, and IBM's Magdo and Magdo.

According to Peltzer's patent, the Fairchild's Isoplanar device 40 as typified by Fig. 4 in his patent has a n-type epitaxial silicon layer 42 formed on a p-type substrate 41. Oxide isolating regions, e.g., 44a, 44b, 44c, and 44d were used

to isolate the different components. Each of these oxide isolating regions has a central flat bottom occupying much chip real estate producing unnecessarily larger devices.

Li's round-bottomed isolating oxide groove 21 of Fig. [21] 2 in 154,300 application improves device leakage current and breakdown voltage. The groove bottom G of zero width eliminates the wasted chip real estate of all other previously existing devices of, e.g., Isoplanar, LOCOS, and oxide-recessed types. This feature produces smaller devices. The oxide isolating regions in this present invention are further narrowed down to even one or two atomic layers occupying the minimum chip real estate. Li's devices also have rounded PN junction peripheral surfaces minimizing contamination by micron-size or even atomic particles thereby increasing yields. See Fig. 2. The smaller the device size, the more critical this yield factor.

In the 154,300 patent application, the device of Fig. 2 is made by thermally growing an oxide groove, band, or material region 21 transversely into a p-type silicon substrate 22. This is followed by oxide-guided, maskless diffusion of n-type dopants from the top surface 23 to give the top n-type silicon layer 24 and the new PN junction region 25. The rounded bottom G has a zero bottom width.

All these devices can still be improved in performance and device size. The present invention provides still better and

further miniaturized solid-state integrated circuits in general and semiconductor integrated circuits in particular.

Specifically, this invention will address the following issues:

1) improving the critical gate layer thickness and structure;

2) reducing the insulating field oxide region size by orders of magnitude from microns to Angstroms;

3) making the entire device more resistant to temperature, stress, impact, vibration, and high-gravity (G) forces due to rapid acceleration and deceleration;

4) simplifying [a] device material inventories and manufacturing process; and

5) providing a new type of high-performance flexible circuits.

and electro-optical telecommunications.

The devices of the invention may use different solid-state or semiconductor materials including Si, Ge, Si-Ge, InP, GaAs, SiC, InAs, superconductor, and diamond. In this invention, Si semiconductor materials are exclusively used by way of illustration. Metal-oxide-semiconductor (MOS) or, in general, conductor-insulator-semiconductor (CIS) devices are used exclusively as examples in this specification. Other types of solid-state and semiconductor circuit devices are also useful.

(3,563,809:14-26-15/4).

Hence, through precise control of beam size and aiming point by, e.g., aligning, focusing, [aligning] or both, ion implantation can control the dimension, shape, and three-dimensional chemical compositions to fractional micron accuracies. Other unique features of implanted ions include:

1) straight penetration without appreciable lateral diffusion to give orders of magnitude sharper boundaries than other conventional methods;

2) controlled size of the implantation region down to less than 1 micron, with an accuracy of 1,000 Angstroms (0.10 microns) down to 10 Angstroms;

3) the ions can be implanted without masking, wet chemistry, and photolithography;

4) the implanted region need not start at the surface of contact with the foreign matter;

5) the shape and three-dimensional chemical composition of the ions can be controlled to fractional micron accuracy; and

6) when used for PN junction or oxide/nitride groove formation, the chemical composition profiles and, in particular, critical PN junction grading, can be of any selected shape, rather than only the exponential or erfc grading obtained with thermal diffusion, respectively for limited or infinite surface diffusion source by thermal diffusion.

intrinsic device of Fig. 3 is shown to have an isolating silicon groove 32, and an upward p-type diffusion from the flat bottom surface formed into the top surface 33 of a slab or wafer of intrinsic semiconductor material 31 (Fig. 3a). This is followed by downward n-type diffusion from the newly grooved surface 32 to produce: [1)]the n-type diffused region 35 [;2)] and an upward p-type diffusion from the planar bottom substrate surface 34 to produce the p-type diffused region 36; [3) the newly formed PN junction region 37] A PN junction region 37 is then formed which is surrounded on all its periphery by isolating intrinsic silicon; [and 4)] the remaining intrinsic isolating slab 31.

The same slab may be alignedly grooved on both the top and bottom intrinsic silicon surfaces to produce the top and the bottom curved surfaces 33 and 34, respectively (Fig. 3b). Next, n-type and p-type dopants are diffused in, from the curvednew top and bottom surfaces, 32 and 34, respectively. The result is a top n-type layer 35, a bottom p-type diffused layer 36, an intermediate striped or pan-cake type PN junction region 37, and the remaining intrinsic isolating material 31.

In both Figs. 3a and 3b, the PN junction region is formed well inside the slab and is completely surrounded by and buried in the electronically inert material 31, without ever being contaminated by atomic or micron-sized dust particles. The same PN junction region can be planar or curved, depending on the shape of the isolating groove and surface concentration of the diffusing n-type and p-type dopants and diffusing times. See

nearly intrinsic silicon material, respectively slightly p and n-type doped. The gate area has a length roughly the same as, but slightly greater than, the prespecified gate length to minimize leakage. In one embodiment, the gate layer can be an oxide/nitride or even an intrinsic silicon material. This intrinsic material can be an equally n-type and p-type doped silicon leaving few uncompensated dopants [producing a] to produce an electrically inert silicon material.

The gate layer 44 may be formed with such a material in such a structure as to be sufficiently yieldable or flexible to minimize effects thereon of thermal mismatch stresses between varying materials of the contacting substrate, pockets, and gate lead. This design significantly improves the performance and reliability of the semiconductor circuit device. With this improved gate layer, the useful life of the old silicon dioxide/nitride material may be extended further into smaller devices.

A pulsed laser system may be used to form this gate insulating layer of an intrinsic silicon. One may use, for example, a 1.5-KW carbon dioxide laser from Convergent Energy, a Q-switched 10-W system from Spectra Physics, or a 3.9 kW to 400-W-average pulsed Nd:YAG laser from Lumonics. The gate layer 44 of the substantially electrically insulating, intrinsic silicon material is centered on the gate area, as shown in Fig. 4, but

Four solutions to this combined thermal and thickness mismatch problem are possible:

1) selecting materials A and B to be as close in chemical composition as possible minimizing differences in thermal coefficients of expansion in the first place;

2) using a gate or field layer material so thin and flexible as to yield and relieve mismatch strains and stresses;

3) forming a curved gate or field layer material which minimizes thermal mismatch stresses through curvature-related stress-relieving mechanisms explained elsewhere and also to be explained shortly; and

4) perfectly chemically or metallurgically bonding materials A and B. This invention uses all these four methods.

Solution (1) is self-evident. Solution (3) will be more fully explained shortly in the formation of the new field insulation layer. For solution (4), please refer to [with reference to] U.S. Patent 5,874,175. This patent discloses techniques to perfectly and strongly bond two materials with widely different coefficients of thermal expansion, even over substantial or large areas and with very thin bonding layers. To understand solution (2), one should briefly review interaction forces between two neighboring atoms. According to the commonly used Leonard-Jones atomic model, the forces between two neighboring atoms have two superimposed force components:

gate layer preventing or minimizing boron penetration, leakage current, and tunneling electrons from the gate to the substrate through the gate oxide. Merely making the new ultra-thin but perfect, curved gate (and field) layers with minimum channel length or gap size (below 20 or 10 nm) may be already [sufficiently] sufficient to improved in device performance and reliability even without the other possible features of this invention such as the atomically liquid-smoothed gate bottom layer of purified, oriented, strengthened or even single-crystalline gate layer material grains as described above.

Making semiconductor integrated circuits is not to achieve scientific perfection, but to rapidly and cost-effectively produce sufficiently good and useful circuits with simple and the minimum processing steps using the least number of processing equipment and device materials. Engineering comprises must be repeatedly made. All relevant technical, financial, and economic considerations must be factored in. Even certain commodity prices, such as of oil, may be an important factor. As a matter of fact, simple minimum processing steps and the least number of processing equipment and device materials in fact invariably lead to higher yield and lower cost, as shown above.

Further, knowing what the desired shape, size, and thickness of the gate layer, methods other than laser heating

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